REMARKS

Summary of Office Action

Claims 1-21 were pending in this application.

Claims 1-21 were rejected under 35 U.S.C. § 103(a) as being obvious from Peng U.S. Patent No. 5,594,675 ("Peng") in view of Ema et al. U.S. Patent Application Publication No. 2002/0130944 ("Ema"). Claim 15 was rejected under 35 U.S.C. § 103(a) as being obvious from Washakowski et al. U.S. Patent Application Publication No. 2005/0238117 ("Washakowski") in view of Ema. Claims 16-21 were rejected under 35 U.S.C. § 103(a) as being obvious from Washakowski and Ema further in view of Peng.

Summary of Applicant's Reply

Applicant has amended claims 1 and 15 and has added new claims 22-25 in order to more particularly define the claimed invention. No new matter has been added. The amendments and new claims are fully supported by the originally-filed application.

Applicant respectfully traverses the Examiner's rejections.

Applicant's Reply to the Prior Art Rejections

Claims 1-21

The Examiner rejected claims 1-21 under 35 U.S.C. § 103(a) as being obvious from Peng in view of Ema. Applicant respectfully traverses this rejection.

Applicant's invention, as defined by amended independent claims 1 and 15, is directed to DSP circuitry that independently processes a plurality of multi-channel data signals. The circuitry includes, inter alia, a column of registers arranged in serial as a sequence of registers and a single input coupled to a register positioned first in the sequence. The circuitry includes interconnection circuitry that allows a value at the single input of each column to be selectively routed to any register in the column by bypassing any register or registers that precede the register in the respective column.

Peng generally describes a digital FIR filter.

Ema generally describes a pulse modulation signal generation circuit 10. A modulation signal generation part 13 is included in the circuit that has a shift register 131 for receiving modulation data in parallel and output serially a pulse sequence. As shown and described in connection with FIG. 14, a LOAD signal causes multiplexers in shift register 131 to either shift data sequentially through registers in the shift register or to store the parallel data received by shift register 131. The multiplexers in the shift register 131 are coupled to different inputs for receiving different portions (i.e., P1, P5, P9 or P13) of the parallel data. (Ema, Abstract, FIG. 14 and ¶¶ 81, 83 and 84.)

The Examiner acknowledges that Peng does not show or suggest bypassing any register or registers that precede said register in said respective column but contends that such implementation is similar to a shift register which is an

obvious matter of design choice and additionally cites Ema as allegedly making up for this deficiency (Office Action, pages 3-4). Applicant respectfully disagrees.

First, applicant respectfully submits that shift register structures do not function to have a value from an input coupled to a register positioned first in a sequence of registers bypass another register in the sequence, as defined by applicant's claims 1 and 15. Instead, shift register structures operate to either shift data in-line when activated or to load parallel data into each of the registers. When data is shifted in-line, the data is moved sequentially from one register to the next and none of the data bypasses any register in the column of registers. In the latter case, for data to be loaded in parallel, multiple inputs, corresponding to different portions of the parallel data are required for loading the value present at each input into a corresponding register of the register column. Thus, it is not the value of the single input coupled to the first register in the sequence of registers that bypasses another register in the sequence or column, but the value at an input coupled to a register positioned later in the sequence that arguably bypasses a previous register in the column. Accordingly, even if one skilled in the art were to modify the Peng device with shift registers (as suggested by the Examiner), one skilled in the art would not arrive at applicant's claimed invention. Therefore, Peng and the suggested modification using shift registers as an obvious matter of design choice does not show or suggest all the features of applicant's claimed invention.

Second, applicant respectfully submits that Ema does not show or suggest having a value from an input coupled to a register positioned first in a sequence of registers bypass another register in the sequence, as defined by applicant's claims 1 and 15. Instead, Ema shows shift registers 131 that have multiple inputs, each associated with a different register in the series of registers 131, required to enable the loading of parallel data (i.e., P1-P13). In Ema, when the load signal is asserted, it is the portion (e.g., P9) of the parallel data (e.g., P13, P9, P5 and P1) that is received by a register positioned later in the sequence (e.g., positioned second in the sequence) that bypasses the other registers in the shift registers 131 and not the value at the single input coupled to the first register in the sequence (e.g., P13). Moreover, the value at the first register in the sequence has to pass through every subsequent register in the sequence to reach a register positioned later in the sequence and thus the value does not bypass any of the subsequent registers in the column. Thus, contrary to the Examiner's assertions, Ema does not make up for the deficiencies of Peng relative to the rejection. Therefore, Peng and Ema, whether taken alone, or in combination, do not show or suggest all the features of applicant's claims.

Accordingly, applicant respectfully submits that independent claims 1 and 15 and claims 2-14 and 16-21 that depend, directly or indirectly from claim 1 or 15, are allowable over the prior art of record.

Claims 15-21

The Examiner rejected claim 15 under 35 U.S.C. § 103(a) as being obvious from Washakowski in view of Ema. The Examiner rejected claims 16-21 under 35 U.S.C. § 103(a) as being obvious from Washakowski and Ema further in view of Peng. Applicant respectfully traverses this rejection.

The Examiner appears to acknowledge that Washakowski does not show or suggest bypassing any register or registers that precede said register in said tap delay line circuitry but contends that such implementation is similar to a shift register which is an obvious matter of design choice and nevertheless cites Ema as allegedly making up for this deficiency (Office Action, pages 9-10).* Applicant respectfully disagrees.

For the reasons stated above with respect to Peng, applicant respectfully submits that Washakowski and the suggested modification using shift registers as an obvious matter of design choice does not show or suggest all the features of applicant's claimed invention. Additionally, as stated above, Ema does not show or suggest having a value from

* The Examiner rejected claim 15 as being obvious from Washakowski in view of Ema (Office Action, page 8). But, in the same rejection, the Examiner stated that "*Peng* did not explicitly show bypassing" and "since the reference *Peng* did not show bypassing... the examiner introduces [EMA]" (Office Action, page 9, ¶¶ 5 and 6, emphasis added). Applicant understands this to mean that Washakowski does not show or suggest bypassing any register or registers that precede said register in said tap delay line circuitry since Peng was not relied upon in the rejection.

an input coupled to a register positioned first in a sequence of registers bypass another register in the sequence and therefore does not make up for the deficiencies of Washakowski in that relative to the rejection.

Peng, cited as allegedly showing features of applicant's dependent claims, does not make up for the deficiencies of Washakowski or Ema relative to the rejection.

Accordingly, applicant respectfully submits that independent claim 15 and claims 16-21 that depend, directly or indirectly therefrom, are allowable over the prior art of record.

New Claims

Applicant has added new claims 22-25 in order to more particularly define the claimed invention. Claims 22-25 depend from allowable claim 1 or 15 and therefore also are allowable. Additionally, applicant respectfully submits that neither Peng, Washakowski nor Ema, whether taken alone or in combination, shows or suggests first and second multiplexer circuits each operative to select between a same first value and a different second value, wherein the same first value is the value received at the input of a register column and the different second value is an output from a register that precedes a register in the column associated with the first or second multiplexer circuits.

Accordingly, applicant respectfully submits that claims 22-25 are patentable over the prior art of record.

Conclusion

The foregoing demonstrates that claims 1-25 are allowable. This application is therefore in condition for allowance. Reconsideration and prompt allowance are accordingly respectfully requested.

Respectfully submitted,

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